What we claim is:

1. A method for testing for the occurrence of bit errors comprising the steps of:

converting and demultiplexing a serial signal for testing purposes into parallel signals corresponding to channels respectively assigned to a plurality of measured devices and a redundant channel;

converting a signal passing through the redundant channel into a channel determination signal for specifying an alignment of the measured devices;

multiplexing output signals of the measured devices and the channel determination signal corresponding to a demultiplexing mode used for demultiplexing the serial signal; and

measuring occurrence of bit errors in the multiplexed signals and detecting measured devices at which the bit errors are generated in consideration of the channel determination signal.

2. The method for testing for the occurrence of bit errors as claimed in claim 1 wherein the channel determination signal comprises a signal in which all bits of the signal passing through the redundant channel are inverted.

3. The method for testing for the occurrence of bit errors as claimed in claim 1 wherein the signal for testing purposes has a pseudo random pattern.

4. A device for testing for the occurrence of bit errors comprising:

a signal generator for generating a serial signal for testing purposes;

a signal demultiplexer for converting and demultiplexing the serial signal into parallel signals corresponding to channels respectively assigned to a plurality of measured devices and a redundant channel;

a channel determination signal generating circuit for converting a signal passing through the redundant channel into a channel determination signal for specifying an alignment of the measured devices;

a signal multiplexer for multiplexing output signals of the measured devices and the channel determination signal corresponding to a

demultiplexing mode of the signal demultiplexer used for demultiplexing the serial signal; and

a bit error measuring device for measuring occurrence of bit errors in output signals of the signal multiplexer and detecting measured devices at which the bit errors are generated in consideration of the channel determination signal.

5. The device for testing for the occurrence of bit errors as claimed in claim 4 wherein the channel determination signal comprises a signal in which all bits of the signal passing through the redundant channel are inverted.

6. The method for testing for the occurrence of bit errors as claimed in claim 2 wherein the signal for testing purposes has a pseudo random pattern.